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Performance Limiting Surface Defects in SiC Epitaxial p-n Junction Diodes

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***Abstract*—Effects of surface defects on performance of kV-class 4H– and 6H–SiC epitaxial p-n junction diodes were investigated. The perimeter recombination and generation, instead of the bulk process, are responsible for forward recombination current and reverse leakage current of the diodes, respectively. Mapping studies of surface morphological defects have revealed that triangular-shaped defects severely degrade high-blocking capability of the diodes whereas shallow round pits and scratch give no direct impact. Device-killing defects in SiC epilayers are discussed based on breakdown voltage mapping. Effective minority carrier lifetimes are mainly limited not by bulk recombination but by perimeter recombination.**

***Index Terms*—Carrier lifetime, high-power device, p-n diode, silicon carbide, surface recombination.**

I. Introduction

UNIQUE potential of silicon carbide (SiC) has been demonstrated in prototype devices projected to high-power, high-frequency, and high-temperature applications [1]–[8]. In spite of recent rapid progress in this field, there still exist many remaining issues to be solved for wide commercial success of SiC technology. For example, performance-limiting factors in SiC devices have scarcely been understood, although micropipes have been claimed to severely degrade high-blocking capability of SiC devices [9]. It is not clear what kind of defects existing in the material itself or being induced during device processing adversely affect the SiC device performance.

In SiC bipolar devices, major mysteries include large leakage current (at least several orders of magnitude higher than simple theoretical prediction) and too fast switching characteristics (short minority carrier lifetime). Concerning SiC p-n junction diodes, high breakdown voltages in the range from 1 to 4.5 kV have been reported for small diodes [3]–[5]. However, detailed analyses on current conduction mechanism and the influence of surface defects on diode performance have not been reported.

In the present paper, the authors investigate the effects of surface defects on the current conduction, breakdown characteristics, and switching behavior of SiC epitaxial p-n junction diodes. Surface recombination and generation processes are revealed to govern major characteristics of p–n diodes. New insights on defects harmful to the diode performance are provided.

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II. Diode Fabrication

4H– and 6H–SiC epitaxial p-n junction diodes were fabricated on $p^+/p/n^-/n$ homoepitaxial layers grown on heavily-doped n-type substrates (production grade) purchased from Cree Research Inc. Epitaxial growth was performed by atmospheric-pressure chemical vapor deposition (CVD) in a SiH_4-C_3H_8-H_2 system. Substrates with 8° (4H–SiC) or 3.5° (6H–SiC) off-angles were used to realize homoepitaxy through step-flow growth (step-controlled epitaxy) [10]. The growth temperature was 1500 °C, at which a growth rate of 4.0 μm/h was obtained. The net donor concentration of 12-μm thick nitrogen (N)-doped n^- epilayers was determined to be 5×10^{14} cm^{-3} for 4H–SiC and 8×10^{14} cm^{-3} for 6H–SiC by capacitance–voltage (C–V) measurements. The doping uniformity over the substrates was about ±6%. The aluminum (Al) acceptor concentrations of a 1.2-μm thick p-layer and a 0.4-μm thick p^+ layer were designed to be 1×10^{18} cm^{-3} and 1×10^{20} cm^{-3}, respectively.

Diodes were processed into a mesa structure with a 6 μm height by reactive ion etching (RIE) using $CF_4 + O_2$ gases with an Al mask. The surface was passivated with 20-nm thick thermal oxides grown by wet oxidation at 1150 °C for 1 h. Contact holes for p^+ layers were formed by wet etching of the oxide with buffered HF. Al/Ti and Ni were employed as ohmic contacts on top p^+ layers and back-side n-type substrates, respectively. Although as-deposited contacts exhibited ohmic characteristics, sintering at 400 °C was made to improve contact resistance and adhesion. The diode size was varied over a wide range from 60 to 1200 μm in diameter to investigate size effects. A schematic illustration of a diode is shown in Fig. 1.

High-resolution current–voltage (I–V) characteristics were measured with a Keithley high-voltage source measure unit 237 in the voltage range up to 1 kV. Above 1 kV, a Sony-Techtronics high-power curve tracer 371A was used. High-voltage reverse current–voltage characteristics were measured by immersing the diodes in Fluorinert™ to avoid air sparking [3]. Switching measurements of the diodes were done with an NF circuit design pulse generator FG-121B and an HP digital oscilloscope 54542C. The peak (maximum) voltage and repetition frequency of the pulses were ±20 V and 1–3 kHz, respectively.

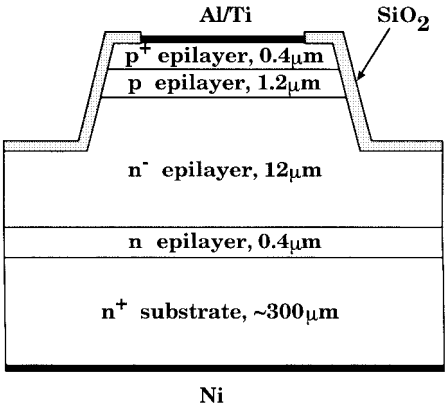

Fig. 1. Schematic illustration of a SiC p-n junction diode.

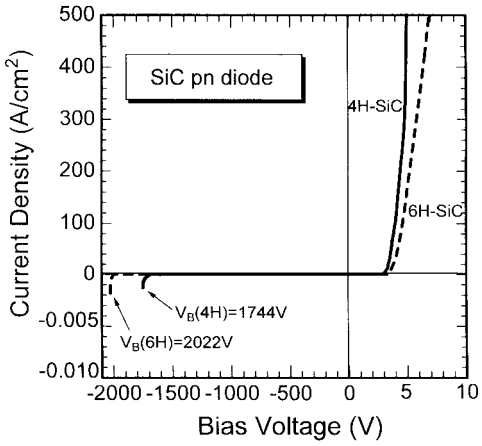

Fig. 2. Linear current J–V characteristics of 100-μmϕ 4H– and 6H–SiC p–n diodes at room temperature.

III. Results and Discussion

A. Basic Performance of p-n Junction Diodes

Room temperature I–V characteristics of 100 μmϕ 4H– and 6H–SiC diodes with the highest breakdown voltages for this diode size are demonstrated in Fig. 2. The 4H–SiC diode exhibited a high breakdown voltage of 1744 V, which is about 80% of the ideal value (2100–2200 V) predicted from the diode structure and breakdown field data [11]. A higher breakdown voltage of 2022 V was achieved for the 6H–SiC diode, probably owing to the slightly higher breakdown field for 6H–SiC [12]. The leakage current density was below 10^{-5} A/cm^2 up to 1.5 kV for 4H–SiC and 1.9 kV for 6H–SiC diodes. All the diodes did not show any physical damage such as crater creation after breakdown. However, when the reverse current density exceeded 0.1–10 A/cm^2 at the breakdown voltage, the diodes showed significantly increased leakage current or were not operational in the subsequent measurements. This degradation may be caused by the lack of proper junction termination, resulting in the electric field crowding at the corners of mesa structures, etc.

A high current density of 500 A/cm^2 could be delivered at forward voltage drops of 4.98 V for 4H–SiC and 6.91 V for 6H–SiC diodes. In the 4H–SiC diode, current conduction above 300 A/cm^2 was limited by a series resistance of 1.09 m

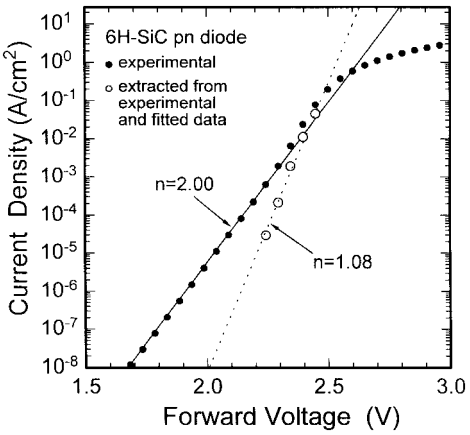

Fig. 3. Semi-logarithmic plot of forward current J–V for an 800-μmϕ 6H–SiC p–n diode at room temperature. Separation of forward current into recombination and diffusion current components is shown.

Ω cm^2, whereas the series resistance of the 6H–SiC diode was 6.05 m Ω cm^2. This better current handling capability of the 4H–SiC diode is expected from much higher electron mobility along the c-axis in 4H–SiC than 6H–SiC [13]. According to the previous report [13], the mobility parallel to the c-axis $(\mu_{\|})$ is only one-third to one-fifth of the mobility perpendicular to the c-axis $(\mu_{\perp})$ in 6H–SiC. 4H–SiC, however, shows an opposite anisotropy: $\mu_{\|}$ is even higher than $\mu_{\perp}$ by 20%. Since $\mu_{\perp}$ of 4H–SiC is two times higher than that of 6H–SiC, about 10 times higher $\mu_{\|}$ can be expected in 4H–SiC.

B. Forward Characteristics

Fig. 3 depicts the semi-logarithmic forward I–V plot of an 800-μmϕ 6H–SiC diode at room temperature. In the low voltage region from 1.6 to 2.2 V, the ideality factor (n) equals 2.00, indicating that carrier recombination dominates the current transport. Above 2.2 V, the gradient of the plot increases with bias voltage before a series resistance comes into effect. The forward current was separated into recombination and diffusion current components, as shown in Fig. 3. First, the recombination current component was determined by the least square fitting of I–V data in the low voltage region by using an equation with $n = 2$. Then, by subtracting the recombination current component from the experimental values denoted by closed circles, open circles, the ideality factor of which equals 1.08 (diffusion current), were obtained. Thus, the current density intercepts were determined to be 5.71×10^{-40} and 7.11×10^{-23} A/cm^2 for diffusion and recombination currents, respectively. Smaller "intercept" current densities of 8.15×10^{-43} (diffusion) and 2.66×10^{-24} A/cm^2 (recombination) were obtained for a 4H–SiC diode with the same mesa size (not shown), mainly due to the lower intrinsic carrier concentration of 4H–SiC $(\sim 10^{-9}$ cm$^{-3})$ than that of 6H–SiC $(\sim 10^{-7}$ cm$^{-3})$.

In general, carrier recombination takes place in the depletion layer (bulk recombination) as well as on the surface or perimeter of a device (surface recombination) [14]. The surface recombination current follows the same bias-voltage dependence as the bulk recombination current, being proportional to $\exp(qV/2kT)$ [14], where q, k, and T are the elemental

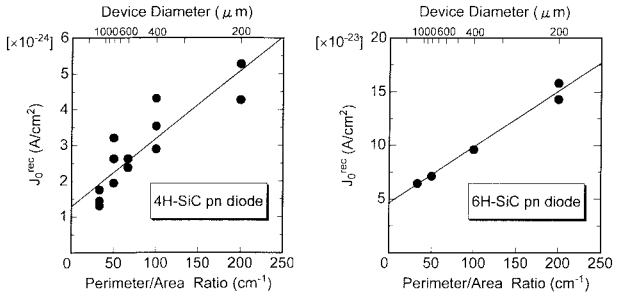

Fig. 4. Perimeter-area (P/A) ratio dependence of the pre-exponential factor of recombination current density determined as the intercept ($J_0^{\rm rec}$) for (a) 4H–SiC and (b) 6H–SiC p–n diodes.

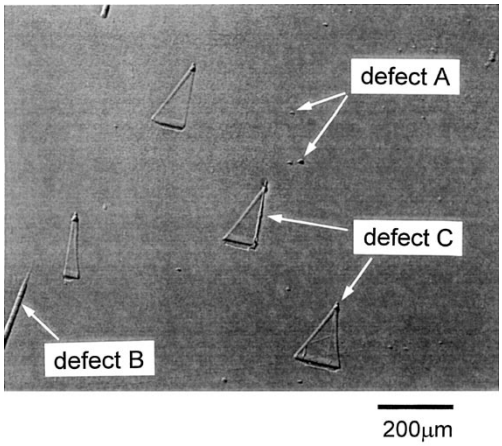

Fig. 5. Typical morphological defects observed on the grown surface: shallow round pit (defect A), "carrot"-like groove (defect B), and triangular-shaped grooves or depression (defect C).

charge, the Boltzmann constant, and the absolute temperature, respectively. Thus, the pre-exponential factor of recombination current $I_0^{\rm rec}$ is given by the sum of these components as follows:

$$I_0^{\rm rec} = \frac{qWv_{\rm th}\sigma N_t n_i}{2}A + qs_pL_sn_iP \qquad (1)$$

assuming one deep trap at midgap. Here

- $v_{\rm th}$ thermal velocity of carriers;
- N_t trap concentration;
- σ capture cross section of the deep trap;
- W effective depletion width where the carrier recombination is significant;
- n_i intrinsic carrier concentration;
- s_p surface (perimeter) recombination velocity;
- L_s surface diffusion length.

The first term in the right side of the equation denotes the bulk recombination current proportional to the diode area A, and the second term the surface recombination current proportional to the perimeter length P. Dividing (1) by area A yields the following equation:

$$\frac{I_0^{\rm rec}}{A} = J_0^{\rm rec} = \frac{qWv_{\rm th}\sigma N_t n_i}{2} + qs_pL_sn_i\frac{P}{A}. \qquad (2)$$

By plotting $J_0^{\rm rec}$ of several diodes with different perimeter-area (P/A) ratios, the contribution of bulk and surface recombination can be distinguished. Fig. 4 represents the P/A ratio dependence of the pre-exponential factor of recombination current density determined as the intercept for (a) 4H–SiC and (b) 6H–SiC diodes at room temperature. The clear P/A ratio dependency reveals that major recombination occurs at the perimeter (sidewall of mesa) and not at the junction interface (bulk), especially in small diodes. From the $J_0^{\rm rec}$ intercept, the pre-exponential factor of bulk recombination current density was estimated to be 1.28×10^{-24} A/cm^2 for 4H–SiC and 4.52×10^{-23} A/cm^2 for 6H–SiC diodes, respectively. The slope of the plot gives the s_pL_s product of 1.2×10^2 cm^2/s for 4H–SiC and 18 cm^2/s for 6H–SiC.

C. Reverse Characteristics

One severe problem which high-power SiC device technology has been facing is that high breakdown voltage can be achieved only for small devices and that breakdown voltage generally decreases with increasing device area. Neudeck *et al.* have reported that micropipes originating from SiC wafers cause pre-avalanche point failure in high-voltage junction devices, being the most harmful defect in SiC materials [9]. The authors have also observed that when SiC p–n or Schottky barrier diodes meet micropipes, most of those diodes exhibit reduced ($30 \sim 50$% lower) breakdown voltage and large leakage current. In some cases, however, a diode without any micropipes breaks down at a reverse voltage much lower than that of a diode containing one or two micropipes. Thus, the relationship between specific defects and high-voltage performance of SiC devices has not been fully elucidated.

To investigate the effects of surface morphological defects on the diode performance, the authors made mapping of morphological defects of SiC epilayers after the mesa-etching process by RIE. Fig. 5 shows typical morphological defects observed on the grown surface: shallow round pit (defect A), "carrot"-like groove (defect B), and triangular-shaped grooves or depression (defect C). Notice that Fig. 5 is not representative of epilayers and most area is much more smooth. The densities of defects A, B, and C are 6×10^3, 70, and 50 cm^{-2}, respectively. Although the formation mechanism of these defects is not made clear, the defects may be created through the disturbance of step flow during epitaxial growth by substrate's defects, particles, etc. [15]–[18]. Another surface defect observed was "scratch" (not shown), which is line-shaped surface damage introduced by a polishing process and is decorated by epitaxial growth. All the diodes investigated in this study are micropipe-free.

Fig. 6 demonstrates the reverse I–V characteristics of several 400 μmϕ 4H–SiC p–n diodes at room temperature. The diodes with defect A or scratch showed very low leakage current, less than 10^{-8}A/cm^2 at -500 V. This current was comparable to that of small diodes (60–200 μmϕ), which contain no visible morphological defects, and was close to a noise level of the present measurement system. No correlation between breakdown voltage and the number of defect A and scratch in each diode was observed, suggesting that defect A and scratch do not give direct impact on the reverse

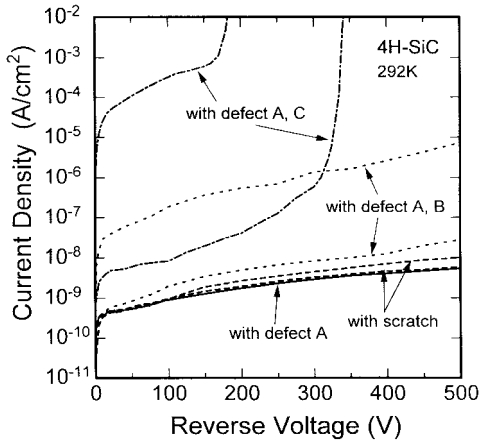

Fig. 6. Reverse current J–V characteristics of several 400 μmϕ 4H–SiC p–n diodes at room temperature. The effects of morphological defects are demonstrated.

characteristics. The breakdown voltage does not depend on the number of defects, but may be limited by the existence of "device-killing defects," even if there is only one. In contrast, the existence of defect B seems to cause the increase in leakage current, and the influence is much more pronounced for defect C. To clarify the influence of morphological defects, histograms of leakage current density at -100 V were made from 43 4H–SiC diodes (400–1200 μmϕ), and are shown in Fig. 7. As can be seen, the defect B and, especially, defect C cause the increase in leakage current. Although some diodes with defect C exhibited rather low leakage current of $10^{-9} \sim 10^{-10}$ A/cm^2 at -100 V, the breakdown voltages of these diodes were significantly lower than average (see Fig. 6). In fact, no diodes which contain defect C could block voltages over 600 V. The large leakage of a few diodes with only defect A may be caused by some other bulk defects which were not visible and not counted in this study. These investigations have revealed that defect C and probably defect B as well should be eliminated to ensure a high production yield of high-power SiC devices.

Though "good" SiC p–n diodes without any defects B and C showed low leakage current, the current level is larger than simple theoretical prediction by more than ten orders of magnitude. As recombination current could be divided into bulk and surface (perimeter) recombination components (Fig. 4), a similar analysis was applied to the leakage current, which is correlated with a carrier-generation process. Fig. 8 depicts the perimeter-area (P/A) ratio dependence of the leakage current density at -100 V of good 4H–SiC diodes without defects B and C at two different temperatures. The leakage current is proportional to the P/A ratio, indicating that the perimeter generation is responsible for the leakage. The almost zero intercept of the plot means that the bulk generation process via deep defect centers is negligible. Heating the diodes resulted in the steeper slope of the plot, due to thermal activation of perimeter generation. Thus, leakage current of SiC diodes may be governed by the perimeter generation, suggesting that surface passivation is a critical issue to reduce the leakage. Wang *et al.* have investigated the carrier generation mechanism in 4H– and 6H–SiC n–p–n storage capacitors from

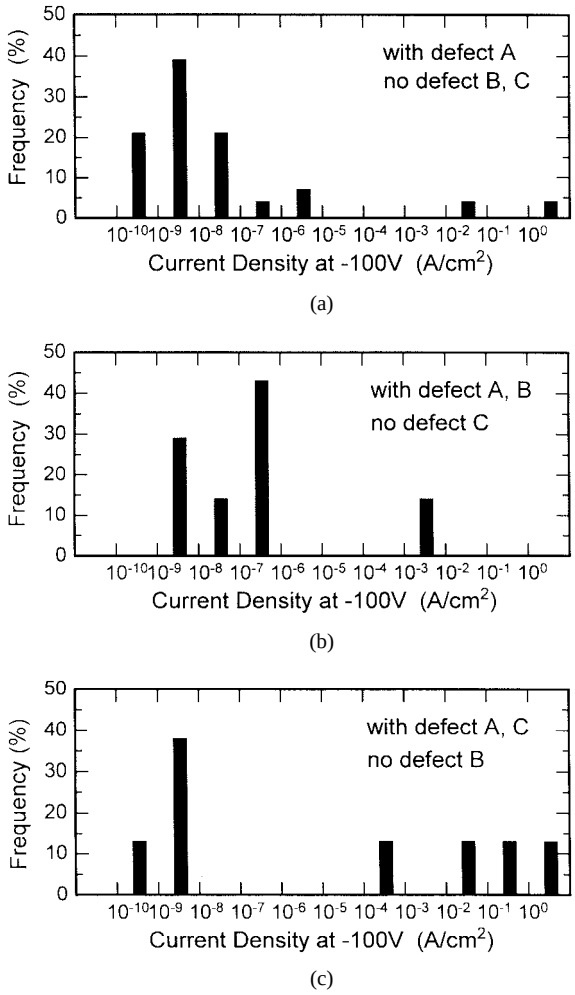

Fig. 7. Histograms of leakage current density at -100 V for 4H–SiC p–n diodes which contain morphological defects of (a) defect A, (b) defects A and B, and (c) defects A and C.

the capacitance recovery transients [19]. From the P/A ratio dependence of the recovery time, three carrier generation mechanisms in the capacitors were identified: bulk, surface and defect-induced generations. They found that defect-induced generation is the most dominant and bulk generation has the smallest contribution. The present study revealed that surface and defect-induced (e.g. defects B and C) generations are also dominating in high-voltage SiC devices.

Fig. 9 shows the diode-area dependence of breakdown voltage for 4H–SiC diodes, obtained from measurements of totally 210 devices. The average, maximum, and minimum breakdown voltages obtained for each size are represented. The breakdown voltage showed rapid decrease when the diode area exceeded 0.5–1 $\times$ 10^{-3} cm^2, which the authors define as the "critical device area." If defects detrimental to high-voltage SiC devices are uniformly distributed, the density of the device-killing defects can be estimated to be 1–2 $\times$ 10^3 cm^{-2}, given as the inverse of the critical device area. This defect density is much higher than a typical micropipe density of 50–100 cm^{-2} observed in commercial production-grade SiC wafers. And it should be reminded that all the diodes measured in this study are micropipe-free. From these facts, the authors conclude that a micropipe is

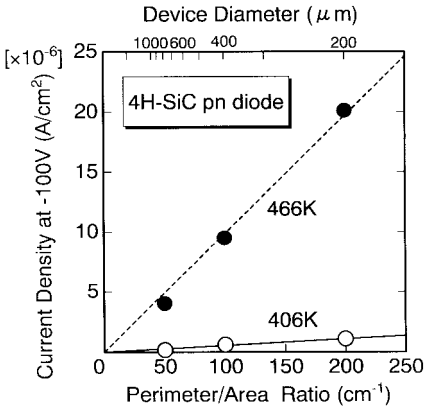

Fig. 8. P/A ratio dependence of the leakage current density at −100 V of good 4H–SiC diodes at two different temperatures. The leakage current is proportional to the P/A ratio, indicating that the perimeter generation is responsible for the leakage.

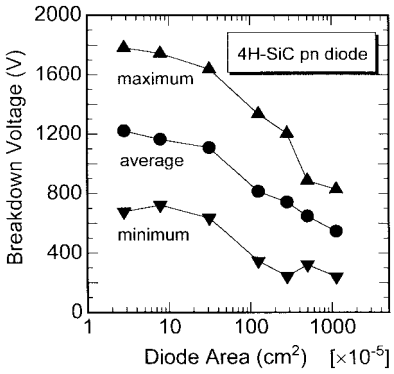

Fig. 9. Diode-area dependence of breakdown voltage for 4H–SiC diodes, obtained from measurements of a total of 210 diodes. The average, maximum, and minimum breakdown voltages obtained for each size are represented.

not the only device-killing defect in SiC material. Chelnokov *et al.* have come to the same conclusion based on device fabrication using micropipe-free Lely platelets [20]. Although the triangular-shaped surface defects (defect C) adversely affect the high-voltage blocking capability as shown in Figs. 6 and 7, the defect density (50 cm^{-2}) is also too low to explain the device-area dependence in Fig. 9. The authors made mapping of breakdown voltage, and tried to correlate the observed breakdown voltage with the type or number of specific morphological defects in each diode, leading to no success except for the clear negative impact of defect C. For example, it is hard to explain the large variation of breakdown voltage (min: 722 V, max: 1744 V) for 100 $\mu m\phi$ diodes, almost all of which are completely morphological defect free. Besides, a 400 $\mu m\phi$ diode with a few tens of defect A and one defect B showed a breakdown voltage (1102 V) higher than several surface-defect free 100 $\mu m\phi$ diodes (800–900 V).

To clarify these puzzling results, detailed correlation between breakdown voltage and bulk defects (dislocation, stacking faults, etc.) as well as passivation is now under investigation. The authors' preliminary etching experiment by molten KOH revealed that the defect C includes a perfect dislocation near the apex of the triangle and partial dislocation pairs at the ends of the triangle base, in good agreement with a recent report [21]. In contrast, defect A seems to be true surface morphological defects created during CVD. A detailed analysis will be published elsewhere.

D. Carrier Lifetime

In high-voltage bipolar devices, a long minority carrier lifetime is crucial to attain effective conductivity modulation and thereby reduced on-state power dissipation. Previous studies on the switching characteristics of SiC p-n junction diodes have shown very short minority carrier lifetimes in the range from 30–80 ns [12], [22], [23]. Recently, Neudeck has pointed out the possibility that perimeter recombination may be responsible for poor effective minority carrier lifetimes in 4H–SiC p^+–n diodes with breakdown voltages of a few hundreds volts [24]. In this study, the authors separate bulk and perimeter contribution to minority carrier lifetimes in kV-class 4H– and 6H–SiC diodes.

The minority carrier lifetimes were determined by a conventional switching analysis of p–n diodes [25]. In the turn-off switching waveform of p–n^- diodes, the storage time τ_s showing relatively constant reverse current is observed, due to the minority carrier (hole in this case) storage in the lightly-doped n^- layer. The minority carrier lifetime τ_p is given by the following equation [25]:

$$\tau_p = \frac{\tau_g}{\left\{\{\mathrm{erf}^{-1}\left(1+\frac{1}{I_R/I_F}\right)\right\}^2}. \tag{3}$$

Here, I_R and I_F are the reverse current during storage time and the forward on-state current, respectively, and erf is the error function. SiC diodes were typically switched from forward bias voltages of +3–4 V with 10–100 A/cm^2 current densities to reverse bias voltages of −10–20 V.

Fig. 10 denotes typical switching characteristics of two 6H–SiC diodes with different diode sizes, showing a longer storage time for a larger diode. Taking account of the effect of perimeter recombination, the minority carrier lifetime estimated from the switching characteristics ("effective hole lifetime") τ_p can be given by [24]

$$\frac{1}{\tau_p} = \frac{1}{\tau} + s_p\frac{P}{A} \tag{4}$$

where τ and s_p are the intrinsic hole lifetime determined by bulk recombination and the surface recombination velocity, respectively. The P/A ratio dependencies of the inverse of effective hole lifetimes $(1/\tau_p)$ for (a) 4H–SiC and (b) 6H–SiC are represented in Fig. 11. The clear P/A ratio dependence of $1/\tau_p$ revealed that perimeter recombination is dominant in small diodes, in agreement with the recent work [24]. From the $1/\tau_p$ intercepts of the plots, the bulk hole carrier lifetimes, which reflect the intrinsic material quality, were determined to be 0.33 μs for 4H–SiC and 0.39 μs for 6H–SiC. This result is encouraging for a few kV device application, because the perimeter recombination will play a smaller role in real high-power switching devices which require large device areas to gain high-current capability. The intrinsic hole lifetimes are, however, still not enough to realize effective conductivity

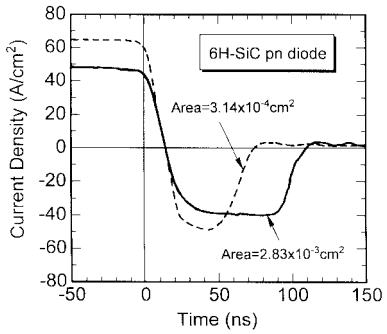

Fig. 10. Typical switching characteristics of two 6H–SiC diodes with different diode sizes, showing a longer storage time for a larger diode.

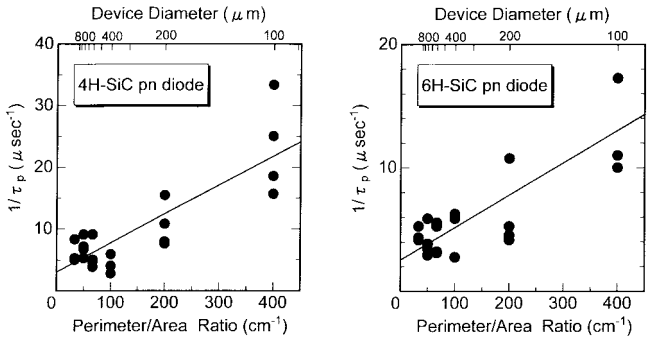

Fig. 11. P/A ratio dependence of $1/\tau_p$ obtained for (a) 4H–SiC and (b) 6H–SiC p–n diodes at room temperature.

modulation in several kV bipolar SiC devices. The slopes of the plot yielded surface recombination velocities of 5×10^4 cm/s for 4H–SiC and 3×10^4 cm/s for 6H–SiC. Thus, polytype dependencies of carrier lifetime and surface recombination velocity seemed to be small. Surface passivation techniques should be improved to reduce the surface recombination effect.

IV. Conclusions

Performance of 4H– and 6H–SiC epitaxial p-n junction diodes with breakdown voltages up to 2 kV was investigated. Forward current could clearly be divided into diffusion and recombination current components, the latter of which was governed by perimeter recombination. Since almost zero intercepts were observed in the P/A ratio dependence of the leakage current, the large leakage in mesa SiC p–n diodes may be caused not by bulk generation via deep defect centers but by carrier generation at the perimeter. Mapping studies of surface morphological defects have revealed that triangular-shaped defects (defect C) and "carrot"-like grooves (defect B) adversely affect the reverse characteristics whereas shallow round pits (defect A) and scratch give no direct impact. Breakdown voltage showed rapid decrease when the diode area exceeded $0.5–1 \times 10^{-3}$ cm^2, suggesting that the density of device-killing defects in the SiC material may be in the range of 10^3 cm^{-2}. Since all the diodes investigated in this study were micropipe-free, a micropipe is not the only device-killing defect in SiC. Effective minority carrier lifetimes were mainly limited by the perimeter recombination instead of bulk recombination.

The present study has demonstrated that surface or perimeter properties can limit SiC device performance, since the material quality of SiC epilayers has been improved to a high level. Surface passivation together with device-structure design may become a critical issue to extract the intrinsic potential of SiC in real devices. Another remaining issue is the identification of device-killing defects and their elimination.

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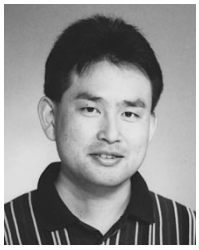
References

[1] D. Allok, B. J. Baliga, and P. K. McLarty, "A simple edge termination for silicon carbide devices with nearly ideal breakdown voltage," *IEEE Electron Device Lett.*, vol. 15, pp. 394–395, Oct. 1994.
[2] A. Itoh, T. Kimoto, and H. Matsunami, "Excellent reverse blocking characteristics of high-voltage 4H–SiC Schottky rectifiers with boron-implanted edge termination," *IEEE Electron Device Lett.*, vol. 16, pp. 139–141, Mar. 1996.
[3] P. G. Neudeck, D. J. Larkin, J. A. Powell, L. G. Matus, and C. S. Salupo, "2000 V 6H–SiC p-n junction diodes grown by chemical vapor deposition," *Appl. Phys. Lett.*, vol. 64, pp. 1386–1388, 1994.
[4] O. Kordina, J. P. Bergman, A. Henry, E. Janzén, S. Savage, J. André, L. P. Ramberg, U. Lindefelt, W. Hermansson, and K. Bergman, "A 4.5 kV 6H silicon carbide rectifier," *Appl. Phys. Lett.*, vol. 67, pp. 1561–1563, 1995.
[5] H. Mitlehner, W. Bartsch, N. Bruckmann, K. O. Dohnke, and U. Weinert, "The potential of fast high voltage SiC diodes," in *Proc. 9th Int. Symp. Power Semiconductor Devices and IC's*, 1997, pp. 165–168.
[6] J. W. Palmour, R. Singh, R. C. Glass, O. Kordina, and C. H. Carter, Jr., "Silicon carbide for power devices," in *Proc. 9th Int. Symp. Power Semiconductor Devices and IC's*, 1997, pp. 25–32.
[7] A. K. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, M. H. White, and C. D. Brandt, "1.1 kV 4H–SiC power UMOSFET's," *IEEE Electron Device Lett.*, vol. 18, pp. 586–588, Dec. 1997.
[8] C. E. Weitzel, J. W. Palmour, C. H. Carter, Jr., K. Moore, K. J. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, "Silicon carbide high-power devices," *IEEE Trans. Electron Devices*, vol. 43, pp. 1732–1740, Oct. 1996.
[9] P. G. Neudeck and J. A. Powell, "Performance limiting micropipe defects in silicon carbide wafers," *IEEE Electron Device Lett.*, vol. 15, pp. 63–65, Feb. 1994.
[10] H. Matsunami and T. Kimoto, "Step-controlled epitaxial growth of SiC: High quality homoepitaxy," *Mater. Sci. Eng.*, vol. R20, pp. 125–166, 1997.
[11] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, "Ionization rates and critical fields in 4H SiC junction devices," *Mater. Sci. Forum*, vol. 264–268, pp. 513–516, 1998.
[12] J. A. Edmond, D. G. Waltz, S. Brueckner, H. S. Kong, J. W. Palmour, and C. H. Carter, Jr., "High temperature rectifiers in 6H–silicon carbide," in *Trans. 1st Int. High Temperature Electron. Conf*, 1991, pp. 207–212.
[13] W. J. Shaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, "Conductivity anisotropy in epitaxial 6H and 4H SiC," in *Mater. Res. Soc. Symp. Proc.*, 1994, pp. 595–600.
[14] C. H. Henry, R. A. Logan, and F. R. Merritt, "The effects of surface recombination on current in $Al_xGa_{1-x}As$ heterojunctions," *J. Appl. Phys.*, vol. 49, pp. 3530–3542, 1978.
[15] J. A. Powell and D. J. Larkin, "Process-induced morphological defects in epitaxial CVD silicon carbide," *Phys. Stat. Sol. (b)*, vol. 202, pp. 529–548, 1997.
[16] A. A. Burk, Jr. and L. B. Rowland, "Homoepitaxial VPE growth of SiC active layers," *Phys. Stat. Sol. (b)*, vol. 202, pp. 263–279, 1997.
[17] C. Hallin, A. O. Konstantinov, O. Kordina, and E. Janzén, "The mechanism of cubic SiC nucleation on off-axis substrates," in *Silicon Carbide and Related Materials 1995*, S. Nakashima, H. Matsunami, S. Yoshida, and H. Harima, Eds. Bristol, U.K.: IOP, 1996, pp. 85–88.
[18] T. Kimoto, "Step-controlled epitaxial growth of α-SiC and device applications," Ph.D. dissertation, Kyoto Univ., Kyoto, Japan, 1995.

[19] Y. Wang, J. A. Cooper, Jr., M. R. Melloch, S. T. Sheppard, J. W. Palmour, and L. A. Lipkin, "Experimental characterization of electron-hole generation in silicon carbide," *J. Electron. Mater.*, vol. 25, pp. 899–907, 1996.
[20] V. E. Chelnokov, A. L. Syrkin, and V. A. Dmitriev, "Overview of SiC power electronics," *Diamond Rel. Mater.*, vol. 6, pp. 1480–1484, 1997.
[21] L. Zhou, P. Pirouz, and J. A. Powell, "Defects in 4H silicon carbide CVD epilayers," in *Mater. Res. Soc. Symp. Proc.*, 1997, pp. 631–636.
[22] M. M. Anikin, A. A. Lebedev, S. N. Pyatko, V. A. Soloviev, and A. M. Strelchuk, "Minority carrier diffusion length in epitaxially grown SiC(6H) p–n diodes," in *Amorphous and Crystalline Silicon Carbide III*, G. L. Harris, M. G. Spencer, and C. Y. Yang Eds. Berlin, Germany: Springer-Verlag, 1992, pp. 269–273.
[23] N. Ramungul, V. Khemka, T. P. Chow, M. Ghezzo, and J. Kretchmer, "Carrier lifetime extraction from a 6H–SiC high-voltage p–i–n rectifier reverse recovery waveform," *Mater. Sci. Forum*, vol. 264–268, pp. 1065–1068, 1998.
[24] P. G. Neudeck, "Perimeter governed minority carrier lifetimes in 4H–SiC p^+n diodes measured by reverse recovery switching transient analysis," *J. Electron. Mater.*, vol. 27, pp. 317–323, 1998.
[25] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Willey-Interscience, 1985, ch. 2.



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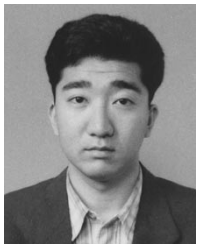

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